AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 1, line 21, as follows:

This delay adjusting circuit includes first-stage to N^{th}[[-]]stage delay elements connected in series to each other and inputted with a clock signal (CLK Input). The delay elements are shown as D1, D2, ···, Dn, D(n+1), ···, DN in a multi-stage structure, wherein N>n, n is a natural number no less than four, and N is a natural number no less than seven.

Please amend the paragraph beginning at page 2, line 4, as follows:

For example, Fig. 2 shows a DLL circuit wherein an initial stage circuit 3 is connected in series to an input side of a delay adjusting circuit 1, and a phase comparing circuit 4 is connected in parallel to an input side of the initial stage circuit 3 and an output side of the delay adjusting circuit 1. In this DLL circuit, assuming that the DLL is locked in one period, it is necessary that a minimum value of the total delay amount [[being]] i.e., the sum of a delay amount of the initial circuit 3 and a delay amount of the delay producing circuit 10 of the delay adjusting circuit 1, be no more than one period. In the foregoing thesis, [[a]] the delay of [[a]] the DLL circuit [[itself]] is set to two periods for coping with a high-speed operation. However, when the delay is large, the number of delay elements increases and a delay variation due to power supply noise [[also]] becomes large [[to]] which increases [[a]] jitter amount~~, and therefore,~~. Therefore it is desirable that the DLL be locked with a delay of one period. Even if [[it]]the DLL circuit is configured that the DLL is locked with a delay of two periods, when the operation is further speeded up, it is necessary to reduce the delay of the DLL circuit itself.

Please amend the paragraph beginning at page 2, line 19, as follows:

As a preferred example of a delay producing circuit [[in]] of the delay adjusting circuit 1, the foregoing thesis describes a structure wherein an even-stage delayed signal and an odd-

HAYES SOLOWAY P.C.
130 W. CUSHING STREET
TUCSON, AZ 85701
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

stage delayed signal are selected from delays of 256 stages. When the delay producing circuit is configured by using 4:1 selectors, each selector selecting one [[from]] out of four inputs to output [[it]], so ~~as to select two~~ that delays from the 256-stage delays are selected, a hierarchical structure is obtained as schematically shown in Fig. 3~~, wherein~~ . Herein the delays are grouped per four stages, and each 4:1 selector selects one from four-stage delays.

Please amend the paragraph beginning at page 2, line 27, as follows:

In ~~case of~~ the foregoing delay adjusting circuit, for the purpose of fully coping with [[the]] an increase in operation frequency required for DLL circuits in recent years, it is necessary to increase the number of delay stages in the delay producing circuit. However, there has been a problem that when the number of delay stages increases, the number of stages (total number) of selectors also increases, and this total number of the selectors ~~resultantly~~ causes an operation slowdown ~~of a basic operation~~ for delay adjustment. For example, in ~~case of~~ the structure shown in Fig. 3, ~~wherein the~~ 256-stage delays are grouped per four stages and the 4:1 selectors are used~~, although an~~ . Although the output of the final stage ~~becomes~~ is one ~~in terms of the number of stages, as is well known to~~ an engineer skilled in circuit design[[,]] would recognize that when 256 transistors are used for delayed output, electrical loads are added [[at]] to power the selectors ~~whose hierarchical number is large, to resultantly slow down~~ thereby slowing the basic operation of the DLL circuit.

Please amend the paragraph beginning at page 3, line 24, as follows:

According to one aspect of the present invention, there is provided a delay producing method using first-stage to N^{th}[[-]]stage delay elements connected in series to each other and, when a clock signal is inputted to an input side of the first-stage delay element, producing an even-stage delayed signal from a clock signal obtained from the even-stage delay element, and

HAYES SOLOWAY P.C.
130 W. CUSHING STREET
TUCSON, AZ 85701
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

an odd-stage delayed signal from a clock signal obtained from the odd-stage delay element. The delay producing method comprises using first-stage and second-stage to N^{th}[[-]]stage selectors arranged in one-to-one correspondence with the delay elements, and each outputting one selected from two inputs, using, as one of inputs to each of the first-stage to N^{th}[[-]]stage selectors, an input to a corresponding one of the delay elements, using, as the other of the inputs to each of the first-stage to $(N-1)^{th}$[[-]]stage selectors, an output from the selector of the next but one stage, outputting the even-stage delayed signal from the first-stage selector, and outputting the odd-stage delayed signal from the second-stage selector.

Please amend the paragraph beginning at page 4, line 10, as follows:

According to another aspect of the present invention, there is provided a delay adjusting method based on the above-mentioned delay producing method ~~according to claim 1,~~ comprising the steps of synthesizing the even-stage delayed clock signal and the odd-stage delayed clock signal with each other and applying a fine adjustment thereto to thereby produce and output an internal clock signal.

Please amend the paragraph beginning at page 4, line 16, as follows:

According to still another aspect of the present invention, there is provided a delay producing circuit including first-stage to N^{th}[[-]]stage delay elements connected in series to each other and, when a clock signal is inputted to an input side of the first-stage delay element, producing an even-stage delayed signal from a clock signal obtained from the even-stage delay element, and an odd-stage delayed signal from a clock signal obtained from the odd-stage delay element. The delay producing circuit comprises first-stage and second-stage to N^{th}[[-]]stage selectors arranged in one-to-one correspondence with the delay elements, and each having two input terminals and one output terminal. In the delay producing circuit, one of the input

HAYES SOLOWAY P.C.
130 W. CUSHING STREET
TUCSON, AZ 85701
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

terminals of each of the first-stage to N^{th}[[-]]stage selectors is connected to an input side of a corresponding one of the delay elements, the other of the input terminals of each of the first-stage to $(N-1)^{th}$[[-]]stage selectors is connected to the output terminal of the selector of the next but one stage, the even-stage delayed signal is outputted from the output terminal of the first-stage selector, and the odd-stage delayed signal is outputted from the output terminal of the second-stage selector.

Please amend the paragraph beginning at page 5, line 9, as follows:

According to still another aspect of the present invention, there is provided a delay producing circuit comprising N-stage delay elements connected in series to each other, and selectors that, in the state where a clock signal is inputted to an input side of the first-stage delay element, switchingly select delays of the given delay elements from input/output portions of the N-stage delay elements in response to a switching control signal from an external control circuit, thereby to output an even-stage delayed clock signal and an odd-stage delayed clock signal. In the delay producing circuit, the selectors are 2:1 selectors each of the type that selectively outputs one from two inputs, and include for-even-stage selectors connected in series to each other so as to successively receive, as one input sequence, an output from the input side of the first-stage delay element, and outputs from output sides of the second-stage to $(N-1)^{th}$-stage delay elements, the outputs each received from every other one of the input/output portions of the N-stage delay elements, and further receive, as the other input sequence, outputs from the second-stage and subsequent selectors at the prior-stage selectors, respectively, thereby to enable the even-stage delayed clock signal obtained by the selector of the stage switchingly selected by the switching control signal, to be outputted through the first-stage selector, and further include for-odd-stage selectors connected in series to each other so as to

HAYES SOLOWAY P.C.
130 W. CUSHING STREET
TUCSON, AZ 85701
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

successively receive, as one input sequence, an output from an output side of the first-stage delay element, and outputs from output sides of the third-stage to N^{th}-stage delay elements, the outputs each received from every other one of the input/output portions of the N-stage delay elements, and further receive, as the other input sequence, outputs from the second-stage and subsequent selectors at the prior-stage selectors, respectively, thereby to enable the odd-stage delayed clock signal obtained by the selector of the stage switchingly selected by the switching control signal, to be outputted through the first-stage selector.

Please amend the paragraph beginning at page 5, line 9, as follows:

According to still another aspect of the present invention, there is provided a delay producing circuit comprising ~~N-stage~~ N^{th} stage delay elements connected in series to each other, and selectors that, in the state where a clock signal is inputted to an input side of the first-stage delay element, switchingly select delays of the given delay elements from input/output portions of the ~~N-stage~~ N^{th} stage delay elements in response to a switching control signal from an external control circuit, thereby to output an even-stage delayed clock signal and an odd-stage delayed clock signal. In the delay producing circuit, the selectors are 2:1 selectors each of the type that selectively outputs one from two inputs, and include for-even-stage selectors connected in series to each other so as to successively receive, as one input sequence, an output from the input side of the first-stage delay element, and outputs from output sides of the second-stage to $(N-1)^{th}$[[-]]stage delay elements, the outputs each received from every other one of the input/output portions of the ~~N-stage~~ N^{th} stage delay elements, and further receive, as the other input sequence, outputs from the second-stage and subsequent selectors at the prior-stage selectors, respectively, thereby to enable the even-stage delayed clock signal obtained by the selector of the stage switchingly selected by the switching control signal, to be outputted

HAYES SOLOWAY P.C.
130 W. CUSHING STREET
TUCSON, AZ 85701
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

through the first-stage selector, and further include for-odd-stage selectors connected in series to each other so as to successively receive, as one input sequence, an output from an output side of the first-stage delay element, and outputs from output sides of the third-stage to N^{th}[[-]]stage delay elements, the outputs each received from every other one of the input/output portions of the ~~N-stage~~ N^{th} stage delay elements, and further receive, as the other input sequence, outputs from the second-stage and subsequent selectors at the prior-stage selectors, respectively, thereby to enable the odd-stage delayed clock signal obtained by the selector of the stage switchingly selected by the switching control signal, to be outputted through the first-stage selector.

Please amend the paragraph beginning at page 6, line 25, as follows:

Referring to Fig. 4, ~~description will be given about~~ a delay adjusting circuit including a delay producing circuit according to a preferred embodiment of the present invention is described.

Please amend the paragraph beginning at page 6, line 28, as follows:

A delay producing circuit 11 includes first-stage to N^{th}[[-]]stage delay elements D1, D2, ···, D(n-1), Dn, D(n+1), D(n+2), ···, DN connected in series to each other, and first-stage and second-stage to N^{th}[[-]]stage selectors S1, S2, S3, Sn, S(n+1), S(n+2), S(n+3), ···, SN that are in one-to-one correspondence with the delay elements D1 to DN. Each of the selectors S1 to SN has two input terminals and one output terminal.

Please amend the paragraph beginning at page 7, line 5, as follows:

One of the input terminals of each of the selectors S1 to S(N-1) is connected to an input side of a corresponding one of the delay elements D1 to DN. The other of the input terminals

HAYES SOLOWAY P.C.
130 W. CUSHING STREET
TUCSON, AZ 85701
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

of each of the selectors S1 to S(N-1) is connected to the output terminal of the selector of the next ~~but one~~ plus one stage.

Please amend the paragraph beginning at page 7, line 9, as follows:

One of the input terminals of the N^{th}[[-]]stage selector SN is connected to an input side of the N^{th}[[-]]stage delay element DN. The other of the input terminals of the N^{th}[[-]]stage selector SN is omitted. In this event, the N^{th}[[-]]stage selector SN will be referred to a specific selecter.

Please amend the paragraph beginning at page 7, line 13, as follows:

The delay producing circuit 11 further includes $(N+1)^{th}$[[-]]stage selector S(N+1). One of the input terminals of the $(N+1)^{th}$[[-]]stage selector S(N+1) is connected to an output side of the N^{th}[[-]]stage delay element DN. The other of the input terminals of the $(N+1)^{th}$[[-]]stage selector S(N+1) is omitted. In this event, the $(N+1)^{th}$[[-]]stage selector S(N+1) will be called a particular selecter.

Please amend the paragraph beginning at page 8, line 7, as follows:

Each of the selectors S1 to S(N+1) is a 2:1 selector of the type that selectively outputs one signal from two inputs. [[The]] One input terminals~~, on one side,~~ of the selectors S1 to S(N+1) are respectively connected to the input side of the first-stage delay element D1, an output side of the second-stage delay element D2, ···, an output side of the $(n-1)^{th}$ delay element D(n-1), an output side of the $(n+1)^{th}$ delay element D(n+1), ···, and an output side of the $(N-1)^{th}$ delay element D(N-1)~~, respectively~~. The other input terminals~~, on the other side,~~ of [[the]] selectors S1 to S(N+1) are each connected to the output terminal of the selector of the next plus [[but]] one stage.

HAYES SOLOWAY P.C.
130 W. CUSHING STREET
TUCSON, AZ 85701
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

Please amend the paragraph beginning at page 8, line 16, as follows:

Further, the delay producing circuit 11 is configured such that delay amounts of the first-stage to N^{th}[[-]]stage delay elements are equal to each other, and the total number of the selectors S1, S3, Sn, ··· for even stages, and the selectors S2, S(n+1), ··· for odd stages becomes N+1 or less.

Please amend the paragraph beginning at page 8, line 20, as follows:

The delay producing circuit 11 in the delay adjusting circuit employs a two-stage selector configuration wherein the 2:1 selectors are used as the for-even-stage selectors and the for-odd-stage selectors, to thereby enable delayed output of the even-stage delayed signal and the odd-stage delayed signal. For example, ~~it is configured that~~ if the n^{th}[[-]]stage selector Sn [[being]] is the for-even-stage selector ~~is inputted with~~ and has inputs that are an output of the [[$(n-1)^{th}$]] $(n)^{th}$[[-]]stage delay element [[D(n-1)]] D(n) and an output of the $(n+2)^{th}$[[-]]stage selector S(n+2), and if the $(n+1)^{th}$[[-]]stage selector S(n+1) [[being]] is the for-odd-stage selector ~~is inputted with~~ and has inputs that are an output of the n^{th}[[-]]stage delay element [[Dn]] D(n+1) and an output of the $(n+3)^{th}$[[-]]stage selector S(n+3). With this configuration, the even-stage delayed signal being the first output can be obtained through the first-stage selector S1, and the odd-stage delayed signal being the second output can be obtained through the second-stage selector S2.

Please amend the paragraph beginning at page 9, line 4, as follows:

When the selectors are arranged in the two-stage selector configuration as described above, the shortest delay path in the delay adjusting circuit in Fig. 4 is a path 1 for feeding the input clock signal (CLK Input) to the selector S1 being the for-even-stage selector from the input side of the delay element D1. Therefore, the smallest delay can be achieved only with a

HAYES SOLOWAY P.C.
130 W. CUSHING STREET
TUCSON, AZ 85701
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

delay of the first-stage selector S1. Even if delays of the other delay elements D2 to DN are added, these are only added ~~succeedingly~~ successively and ~~thus give no influence to~~ do not influence the smallest delay obtained by the shortest delay path.

Please amend the paragraph beginning at page 9, line 18, as follows:

In the basic operation, an even-stage delayed clock signal (Even) and an odd-stage delayed clock signal (Odd) are outputted from the delay producing circuit 11. It is assumed that the delay adjusting circuit including the delay producing circuit 11 is applied to a DLL circuit. If a locking position of the DLL is delayed when delays of the delay elements Dn and D(n+1) are selected at the selectors S(n+1) and S(n+2), respectively, by a switching control signal from the exterior, then the delay elements D(n+2) and D(n+1) are selected [[at]] by the selectors S(n+3) and S(n+2), respectively, by a switching control signal from the exterior, then the delay elements D(n+2) and D(n+3) are selected [[at]] by the selectors S(n+3) and S(n+4), respectively, by a switching control signal from the exterior, and then likewise, so that an even-stage delayed signal and an odd-stage delayed signal are switched alternately therebetween.

Please amend the paragraph beginning at page 10, line 1, as follows:

In this event, at the outset, the first-stage selector S1 of the for-even-stage selectors and the first-stage selector S2 of the for-odd-stage selectors select the delay element side (side A), while the other selectors S3 to S6 select the selector output side (side B). As a result, a delay of an even-stage delayed signal becomes ts, and a delay of an odd-stage delayed signal becomes ts+td.

Please amend the paragraph beginning at page 10, line 7, as follows:

Then, the first-stage selector S2 of the for-odd-stage selectors and the second-stage selector S3 of the for-even-stage selectors select the delay element side (side A), while the

HAYES SOLOWAY P.C.
130 W. CUSHING STREET
TUCSON, AZ 85701
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

other selectors S1 and S4 to S6 select the selector output side (side B). As a result, a delay of an even-stage delayed signal becomes 2ts+2td, and a delay of an odd-stage delayed signal becomes ts+td.

Please amend the paragraph beginning at page 10, line 13, as follows:

Further, the second-stage selector S3 of the for-even-stage selectors and the second-stage selector S4 of the for-odd-stage selectors select the delay element side (side A), while the other selectors S1, S2, S5, and S6 select the selector output side (side B). As a result, a delay of an even-stage delayed signal becomes 2ts+2td, and a delay of an odd-stage delayed signal becomes 2ts+3td.

Please amend the paragraph beginning at page 10, line 19, as follows:

Subsequently, the second-stage selector S4 of the for-odd-stage selectors and the third-stage selector S5 of the for-even-stage selectors select the delay element side (side A), while the other selectors S1 to S3 and S6 select the selector output side (side B). As a result, a delay of an even-stage delayed signal becomes 3ts+4td, and a delay of an odd-stage delayed signal becomes 2ts+3td.

Please amend the paragraph beginning at page 11, line 1, as follows:

It is assumed that the foregoing delay adjusting circuit is applied to the DLL circuit shown in Fig. 2. In this case, if it is attempted to cover a low speed up to about 10ns, the number of stages of delay elements becomes large. In case of N stages, a delay of the initial circuit 3 + N x td + N x ts is a maximum value for locking the DLL circuit. If a larger [[more]] delay is required, it is necessary to increase the number of stages (total number) of delay elements.

HAYES SOLOWAY P.C.
130 W. CUSHING STREET
TUCSON, AZ 85701
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

Please amend the paragraph beginning at page 11, line 7, as follows:

On the other hand, resolution required for the DLL circuit may be lower at low periods. Accordingly, although the delay amounts td of the delay elements D1 to DN are [[set]] equal to each other, in the foregoing embodiment, they may have different delays ~~amounts~~.

Please amend the paragraph beginning at page 11, line 25, as follows:

According to the delay adjusting circuit described above, the minimum value of the delay can be set to only the delay amounts of each selector to thereby achieve [[the]] high-speed operation. Further, the delay elements and the selectors can be configured in one-to-one correspondence with each other so ~~that no influence is given to~~ the minimum value of the delay has no influence. Therefore, even if the number of delay stages and the number of selector stages are increased, the delay at the selectors can be minimized to enable the stable and speedy operation. Further, by configuring the delay elements to have different delay amounts in the delay producing circuit, it is possible to also deal with the low periods without increasing the number of stages (total number) of the delay elements.

HAYES SOLOWAY P.C.
130 W. CUSHING STREET
TUCSON, AZ 85701
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567